Amendments to the Abstract:

Please replace paragraph **[41]** with the following amended paragraph:

[41] A non-volatile memory cell includes a first insulating layer over a substrate region, and a floating gate. The floating gate includes a first polysilicon layer over the first insulating layer and a second polysilicon layer over and in contact with the first polysilicon layer. The first polysilicon layer has a predetermined doping concentration and the second polysilicon layer has a doping concentration which decreases in a direction away from an interface between the first and second polysilicon layers. A second insulating layer overlies and is in contact with the second polysilicon layer. A control gate includes a third polysilicon layer over and in contact with the second insulating layer, and a fourth polysilicon layer over and in contact with the third polysilicon layer. The fourth polysilicon layer has a predetermined doping concentration, and the third polysilicon layer has a doping concentration which decreases in a direction away from an interface between the third and fourth polysilicon layers. ~~In accordance with an embodiment of the present invention, a semiconductor structure includes an undoped polysilicon layer, a doped polysilicon layer in contact with the undoped polysilicon layer, and an insulating layer in contact with the undoped polysilicon layer. The undoped polysilicon layer is sandwiched between the doped polysilicon layer and the insulating layer. a first insulating layer over a substrate region.~~